Active Project (2016 - 2016)

Bringing 3D Memory Cubes to Space: a "Rad-Hard by Design Study" with an Open Architecture, Phase I Project

SBIR/STTR Programs | Space Technology Mission Directorate (STMD)

ABSTRACT

The computing capabilities of onboard spacecraft are a major limiting factor for accomplishing many classes of future missions. Although technology development efforts are underway that will provide improvements to spacecraft CPUs, they do not address the limitations of current onboard memory systems. In addition to CPU upgrades, effective execution of data-intensive operations such as terrain relative navigation, hazard detection and avoidance, autonomous planning and scheduling, and onboard science data processing and analysis require high-bandwidth, low-latency memory systems to maximize processor usage (the memory wall) and provide rapid access to observational data captured by high-data-rate instruments (e.g., Hyperspectral Infrared Imager, Interferometric Synthetic Aperture Radar). 3D ICs, after a long wait, is now a reality. The first mainstream product is 3D memory cubes, where multiple memory tiers (4 DRAM tiers as of 2015) are vertically integrated to offer manifold improvement in size, capacity, speed, and power consumption compared with 2D counterparts. Indeed, these are the memory parts that will truly enable aforementioned missions. Unfortunately, none of these are ready for space. The purpose of this research is to investigate the challenges and opportunities in deploying 3D memory cubes into space missions.

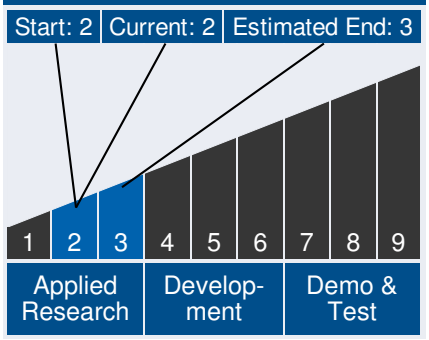
ANTICIPATED BENEFITS

To NASA funded missions:

Potential NASA Commercial Applications: In order to effectively address the SWaP constraints of space hardware, it is desired to compact the electronics to as small a size as possible. Advances in the arena of 3D stacking and 3D ICs have opened a window of opportunity to integrate these types of packaging for space applications. Very high density, high bandwidth, RAD-hard reliable memory cubes would address some of the immediate needs for space applications. The one drawback is

Table of Contents

Technology Maturity



Management Team

Program Executives:

- Joseph Grant
- Laguduva Kubendran

Program Manager:

- Carlos Torrez

Continued on following page.

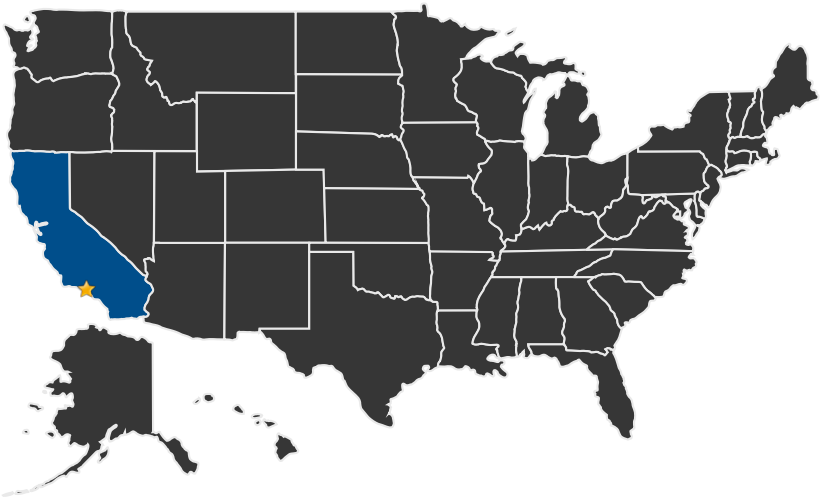
Bringing 3D Memory Cubes to Space: a "Rad-Hard by Design Study" with an Open Architecture, Phase I Project

the ready availability of this type of space qualified 3D hardware. The proposed 3D RAD-hard memory stack will be directly applicable to space electronics requiring memory intensive applications. The technology derived from this study will allow NASA to utilize this on a broader range of capabilities that can be brought to space.

To the commercial space industry:

Potential Non-NASA Commercial Applications: Optimization of the logic base of any memory cube type has not been available for any application. Development of the design tools to achieve better optimization of these logic bases will in turn lead to a broader application base which will benefit not only the users for space applications, but will benefit terrestrial users to help improve the efficiency of their electronics by addressing SWaP issues.

U.S. WORK LOCATIONS AND KEY PARTNERS



U.S. States With Work

Lead Center:
Jet Propulsion Laboratory

Management Team *(cont.)*

Principal Investigator:
- James Yamaguchi

Technology Areas

Primary Technology Area:
Modeling, Simulation, Information Technology and Processing (TA 11)
- Computing (TA 11.1)
  - Flight Computing (TA 11.1.1)

Other Organizations Performing Work:

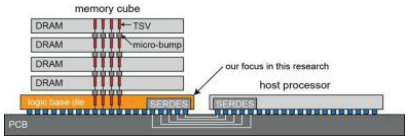
- Irvine Sensors Corporation (Costa Mesa, CA)

PROJECT LIBRARY

Presentations

- Briefing Chart
  - (http://techport.nasa.gov:80/file/23369)

IMAGE GALLERY



Bringing 3D Memory Cubes to Space: a "Rad-Hard by Design Study" with an Open Architecture, Phase I

DETAILS FOR TECHNOLOGY 1

Technology Title

Bringing 3D Memory Cubes to Space: a "Rad-Hard by Design Study" with an Open Architecture, Phase I

Potential Applications

In order to effectively address the SWaP constraints of space hardware, it is desired to compact the electronics to as small a size as possible. Advances in the arena of 3D stacking and 3D ICs have opened a window of opportunity to integrate these types of packaging for space applications. Very high density, high bandwidth, RAD-hard reliable memory cubes would address some of the immediate needs for space applications. The one drawback is the ready availability of this type of space qualified 3D hardware. The proposed 3D RAD-hard memory stack will be directly applicable to space electronics requiring memory intensive applications. The technology derived from this study will allow NASA to utilize this on a broader range of capabilities that can be brought to space.